



NM70-I

V:1.0

SCHEMATICS TABLE:

Page	Index	Page	Index
1	Cover Page	16	CONN-HDMI/DVI/SATA
2	Block Diagram	17	SIO-F71869E
3	CPU-DMI/FDI/PEG	18	PCIE LAN - RTL8105E/8111E
4	CPU-CLK/MISC/JTAG	19	AUDIO Part A - VT1705CF
5	CPU-DDR3	20	AUDIO Part B - Panel
6	CPU-POWER/VCORE/VT	21	CONN-LPT / COM / PSKBM
7	CPU-POWER/Graphy/Gnd	22	DC/DC VCORE/VAXG-RT8167
8	DDR3 SODIMM	23	DC/DC CPUVTT/VSA/1.05V
9	PCH- HDA/JTAG/SPI/SATA	24	DC/DC VDIMM/1.8V/DDRVT/EUP
10	PCH-PCIE/SMBUS/CLK	25	PCIEX16 Slot
11	PCH-DMI/FDI/GPIO/MISC	26	Front Panel,FAN,PowerConn
12	PCH-VGA/LVDS/DP	27	GPIO
13	PCH-USB/PCI	28	Power Delivery Chart
14	PCH-POWER	29	Power Sequencing Diagram
15	PCH-GND	30	Clock Distribution

REVISION HISTORY:

Rev	Date	Notes
A	06-04-2012	INITIAL RELEASE Modify form CDC-I
B	08-10-2012	1) 導入5VDUAL取代5VSB 2) Del D3 改MN13 3)SIO#85 POWER 為VBAT 4))修正SATA4 (Port0 TX NP接反) 5)Page28 RT8121更換成RT8140 6) reanme ER14->R21 ME_LOCK1->ME_LOCK BT1->BT CODEC1 7)SATA1->SATA3;SATA2->SATA4;SATA3->SATA2;SATA4->SATA1
PCB	15-ES1-010010	
NM70	01-201-070091	
847	01-152-110021	
807	01-149-150092	
VT1705CF	02-301-705622	
NCT3914	02-415-941900	
LVDS	10-262-030132	
	10-262-030331	
RTL8105E-VL-CG	01-267-105352	
RTL8111E-VL-CG	01-267-111357	
RT8167AGQW	02-437-167790	
PCIEX16	10-455-164030	
SPI ROM SOCKET	11-127-008120	
DIMM	11-025-204123	
220P-VPORT	04-140-221005	

待改

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example 1) DESIGN NOTES in text for the design note to grey are information show the note inside the notes.
colored box.

DESIGN NOTE: Example 2) DESIGN NOTES in text for the design note to yellow are notes of show the note inside the caution.
colored box.

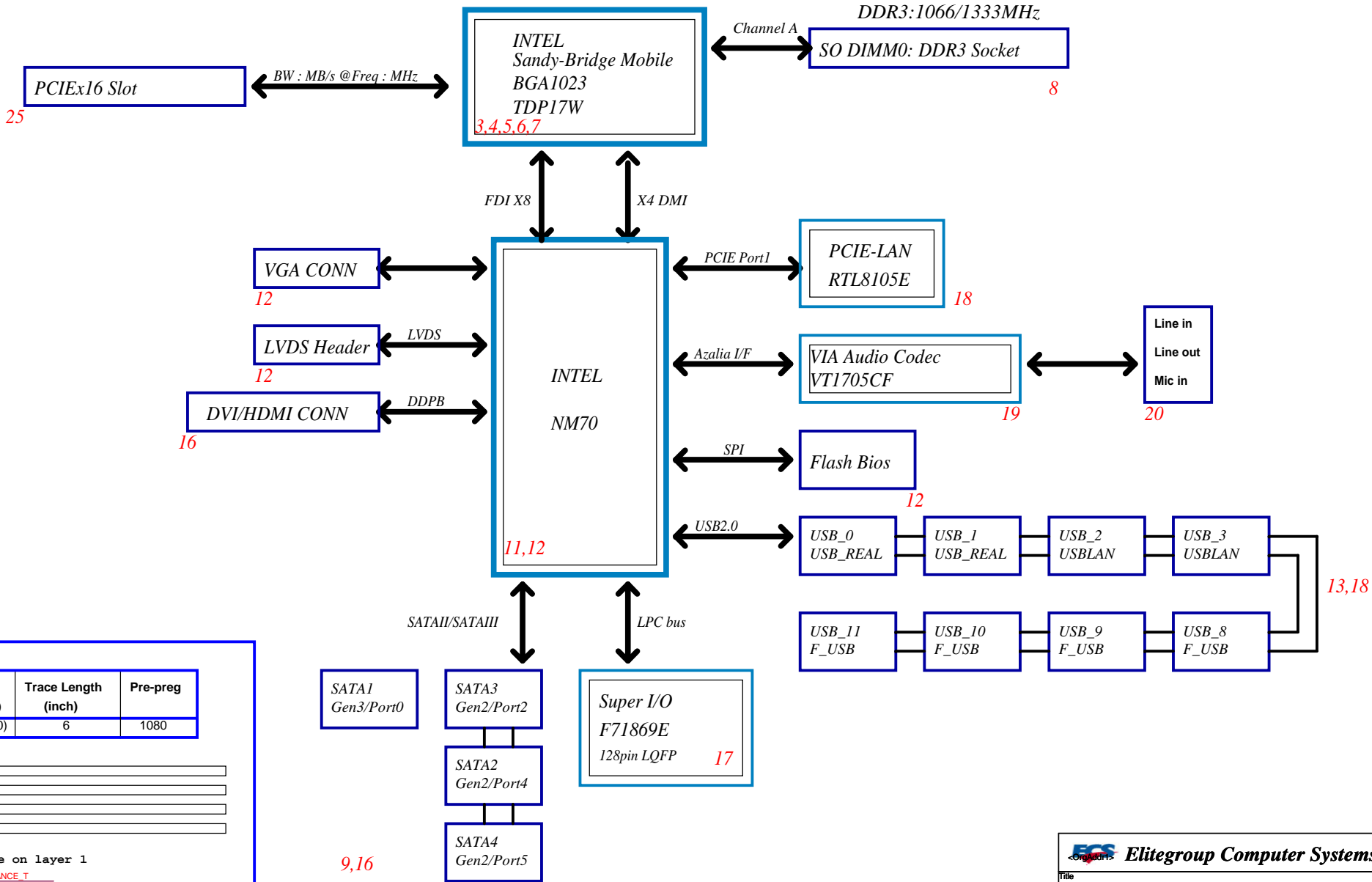
DESIGN NOTE: Example 3) DESIGN NOTES in text for the design note to red are critical, and show the note inside the must be understood and followed.
colored box.

PCB : 170 x 170 mm ; 4 layers
PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

Elitegroup Computer Systems		
Title		
Cover Page		
Size	Document Number	Rev
Custom	NM70-I	1.0
Date:	Tuesday, August 21, 2012	Sheet 1 of 30

VCORE POWER
PWM
VRD12/IMVP7
(RT8167)

21



PCB Impedance control

Impedance (OHM)	Trace Width (mil)	Trace Length (S/W/S)	Trace Length (inch)	Pre-preg
50	4	(50/4/50)	6	1080

PCB STACK:

Layer 1: TOP

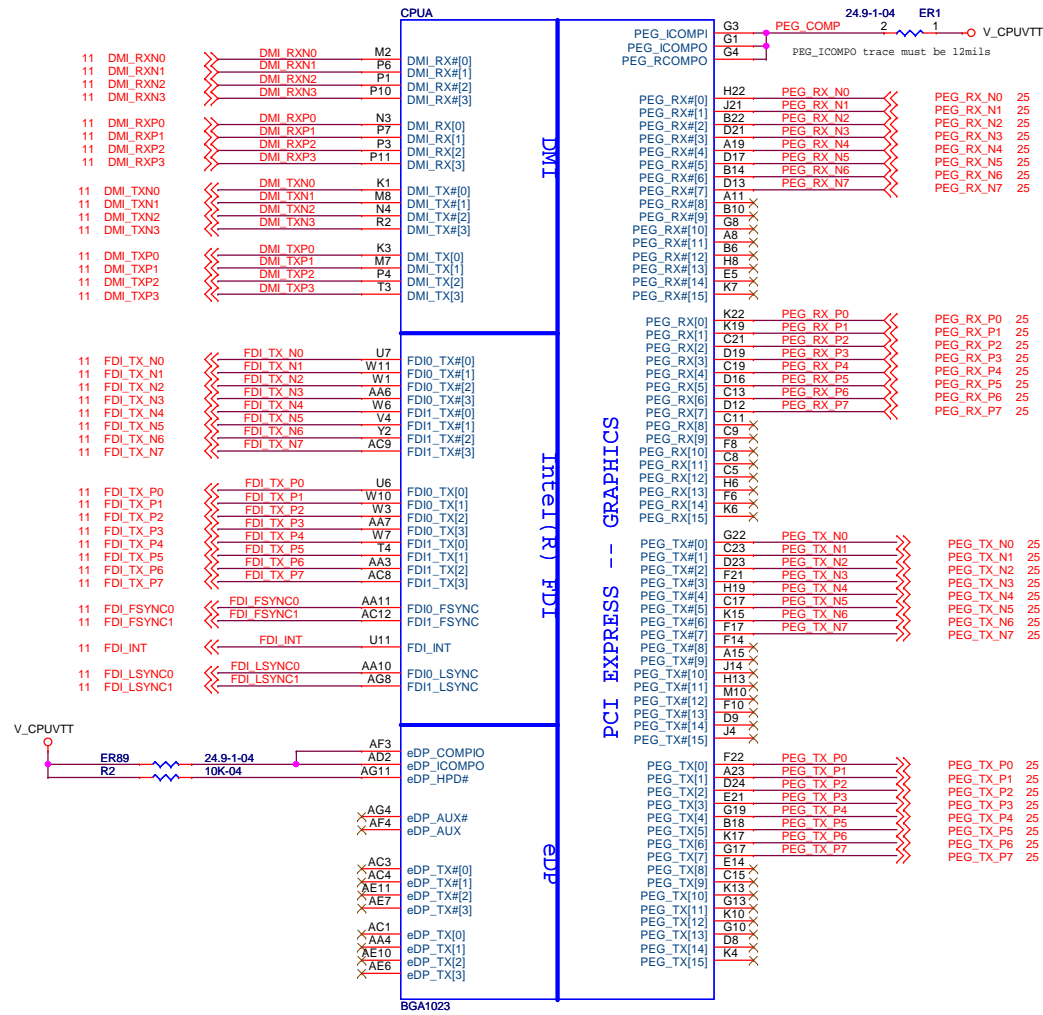
Layer 2: PWR

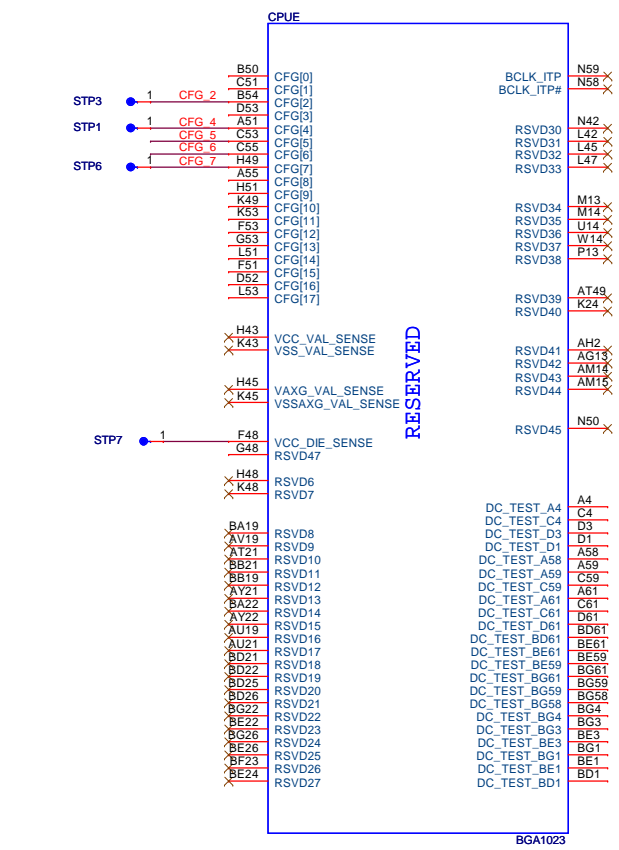
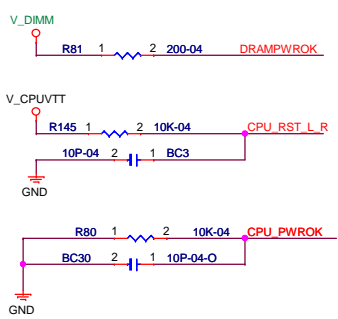
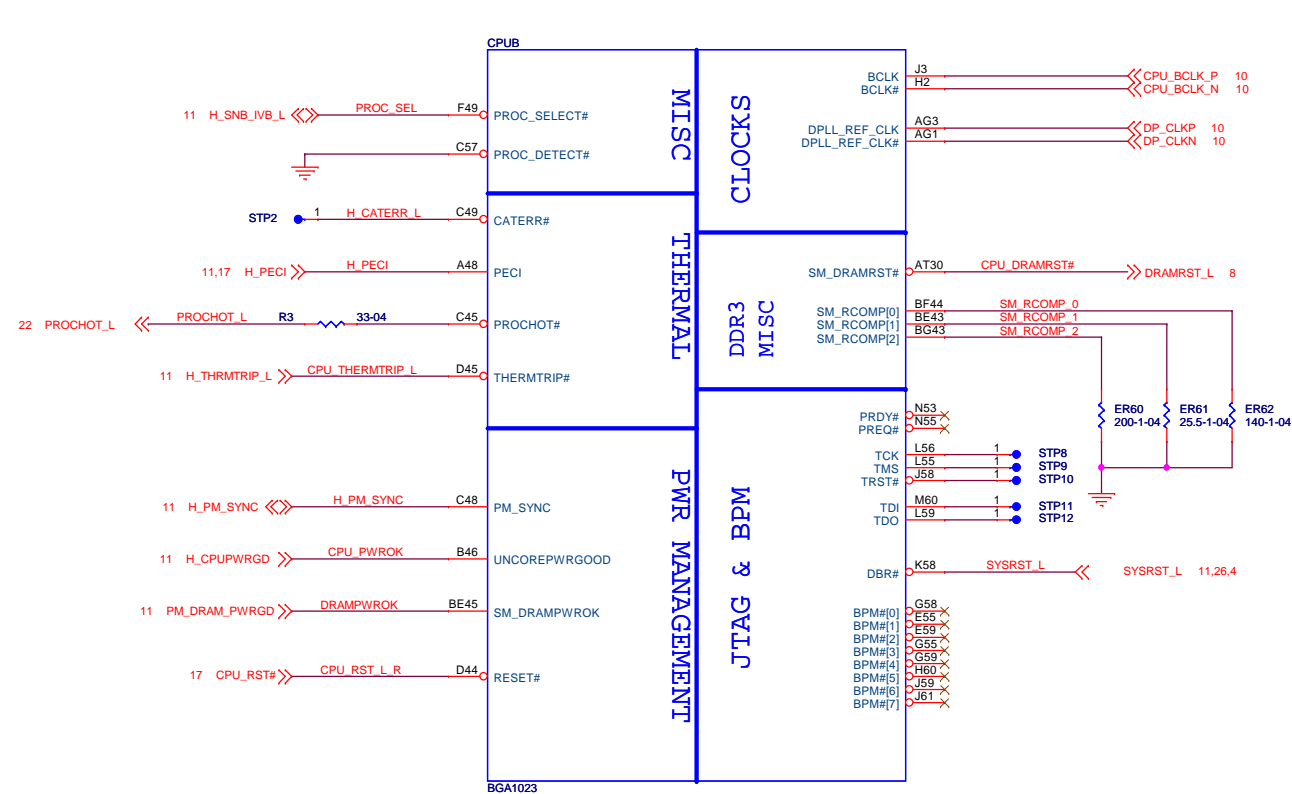
Layer 3: GND

Layer 4: BOTTOM

Trace on layer 1

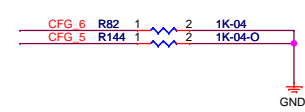
Trace on layer 4

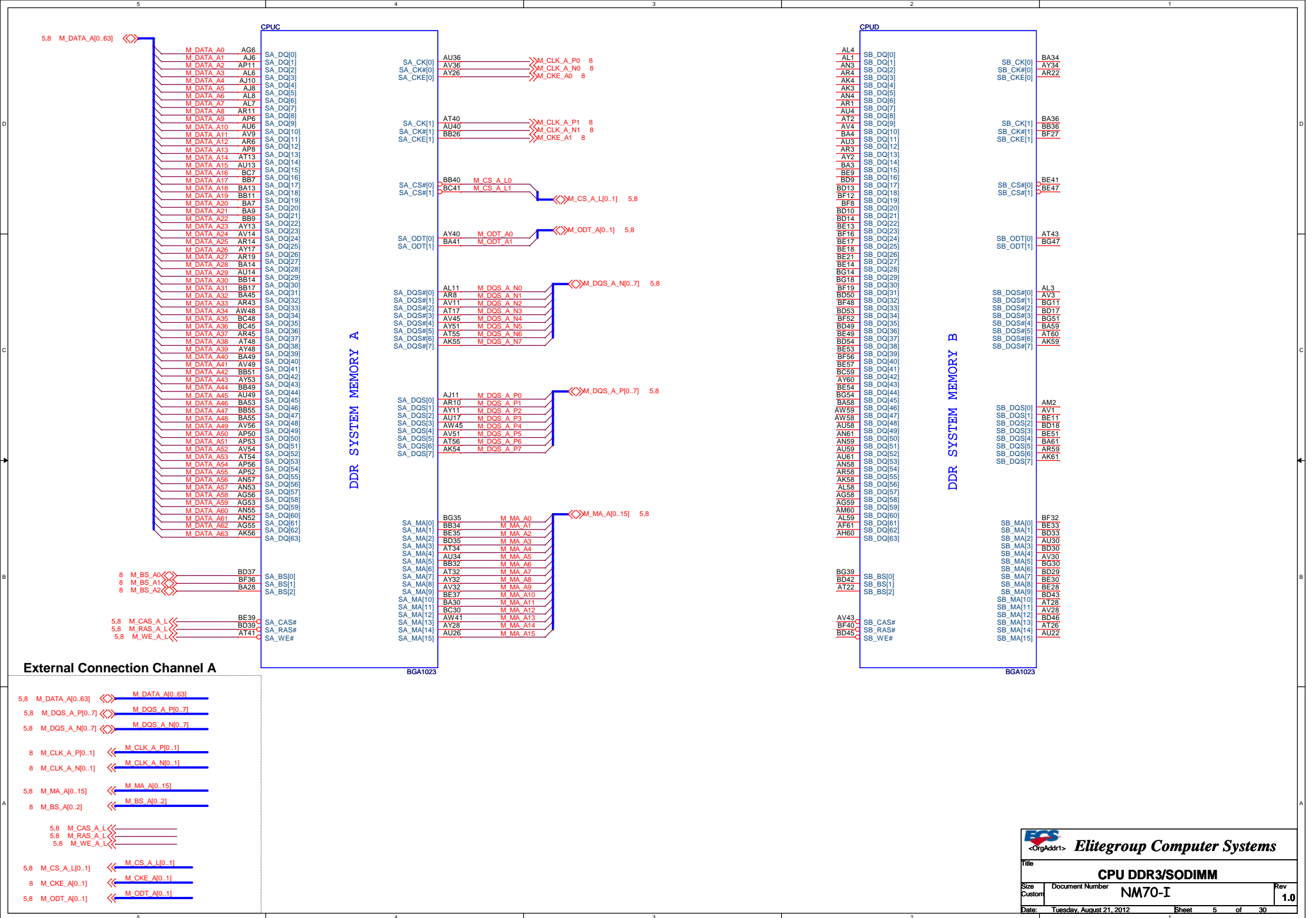




CFG[0..17] have internal Pull-High

	CFG	Stauts	DESCRIPTION
PCI Express Reversal	2	1	Normal
		0	reversed
EDP Enable	4	1	Disable
		0	Enable
PCI Express Bifurcation	5 6	1 1	x16 *1
		1 0	x8*2





POWER

CPUF

VCORE
21.5A

A26 VCC[1]
A29 VCC[2]
A31 VCC[3]
A34 VCC[4]
A35 VCC[5]
A38 VCC[6]
A39 VCC[7]
A42 VCC[8]
C26 VCC[9]
C27 VCC[10]
C32 VCC[11]
C34 VCC[12]
C37 VCC[13]
C39 VCC[14]
C42 VCC[15]
D27 VCC[16]
D32 VCC[17]
D34 VCC[18]
D37 VCC[19]
D39 VCC[20]
D42 VCC[21]
E26 VCC[22]
E28 VCC[23]
E32 VCC[24]
E34 VCC[25]
E37 VCC[26]
E38 VCC[27]
F25 VCC[28]
F26 VCC[29]
F28 VCC[30]
F32 VCC[31]
F34 VCC[32]
F37 VCC[33]
F38 VCC[34]
F42 VCC[35]
G42 VCC[36]
H25 VCC[37]
H26 VCC[38]
H28 VCC[39]
H29 VCC[40]
H32 VCC[41]
H34 VCC[42]
H35 VCC[43]
H37 VCC[44]
H38 VCC[45]
H40 VCC[46]
J25 VCC[47]
J26 VCC[48]
J28 VCC[49]
J29 VCC[50]
J32 VCC[51]
J34 VCC[52]
J35 VCC[53]
J37 VCC[54]
J38 VCC[55]
J40 VCC[56]
J42 VCC[57]
K26 VCC[58]
K27 VCC[59]
K29 VCC[60]
K32 VCC[61]
K34 VCC[62]
K35 VCC[63]
K37 VCC[64]
K39 VCC[65]
K42 VCC[66]
L25 VCC[67]
L28 VCC[68]
L33 VCC[69]
L36 VCC[70]
L40 VCC[71]
N26 VCC[72]
N30 VCC[73]
N34 VCC[74]
N38 VCC[75]
VCC[76]

CORE SUPPLY

PEG IO AND DDR IO

V_CPUVTT
8A MAX
AF46
AG48
AG50
AG51
AJ17
AJ21
AJ25
AJ28
AJ43
AJ47
AJ50
AK50
AK51
AL14
AL16
AL15
AL16
AL16
AL20
AL22
AL26
AL45
AL48
AM16
AM17
AM21
AM43
AM47
AN20
AN22
AN42
AN45
AN48
VCCIO[1]
VCCIO[3]
VCCIO[4]
VCCIO[5]
VCCIO[6]
VCCIO[7]
VCCIO[8]
VCCIO[9]
VCCIO[10]
VCCIO[11]
VCCIO[12]
VCCIO[13]
VCCIO[14]
VCCIO[15]
VCCIO[16]
VCCIO[17]
VCCIO[18]
VCCIO[19]
VCCIO[20]
VCCIO[21]
VCCIO[22]
VCCIO[23]
VCCIO[24]
VCCIO[25]
VCCIO[26]
VCCIO[27]
VCCIO[28]
VCCIO[29]
AA14
AA15
AB17
AB20
AC13
AD16
AD18
AD21
AE14
AE15
AF16
AF18
AF20
AG15
AG16
AG17
AG20
AG21
AJ14
AJ15
VCCIO[30]
VCCIO[31]
VCCIO[32]
VCCIO[33]
VCCIO[34]
VCCIO[35]
VCCIO[36]
VCCIO[37]
VCCIO[38]
VCCIO[39]
VCCIO[40]
VCCIO[41]
VCCIO[42]
VCCIO[43]
VCCIO[44]
VCCIO[45]
VCCIO[46]
VCCIO[47]
VCCIO[48]
VCCIO[49]

V_CPUVTT
W16
W17
VCCIO_SEL
BC22
VCCIO_SEL
STP24
V_CPUVTT
AM25
AN22

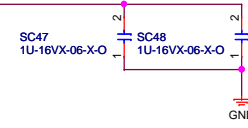
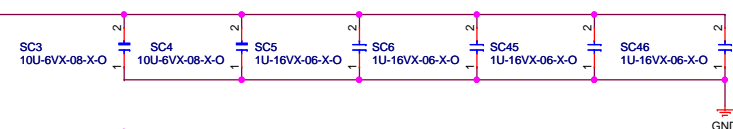
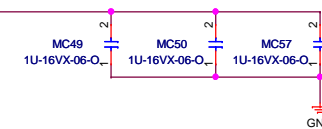
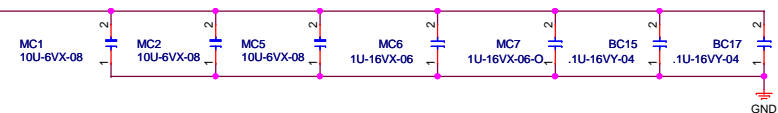
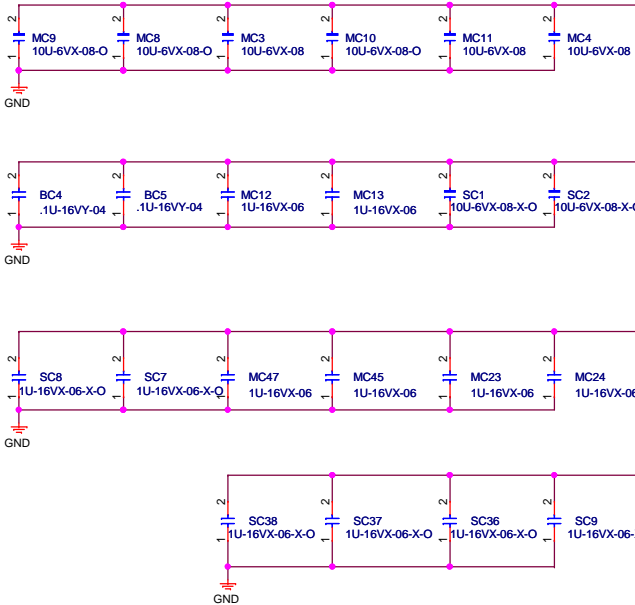
QUIET
RAILS

SVID

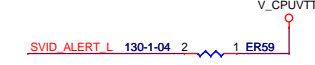
SENSE LINES

A44 SVID_ALERT_L SVID_ALERT_L 22
B43 SVID_CLK SVID_CLK 22
C44 SVID_DATA SVID_DATA 22
F43 VCC_CPUSENSE VCC_CPUSENSE 22
G43 VSS_CPUSENSE VSS_CPUSENSE 22
AN16 VCCIO_SEN VCCIO_SEN 23
AN17 VSSIO_SEN VSSIO_SEN 23

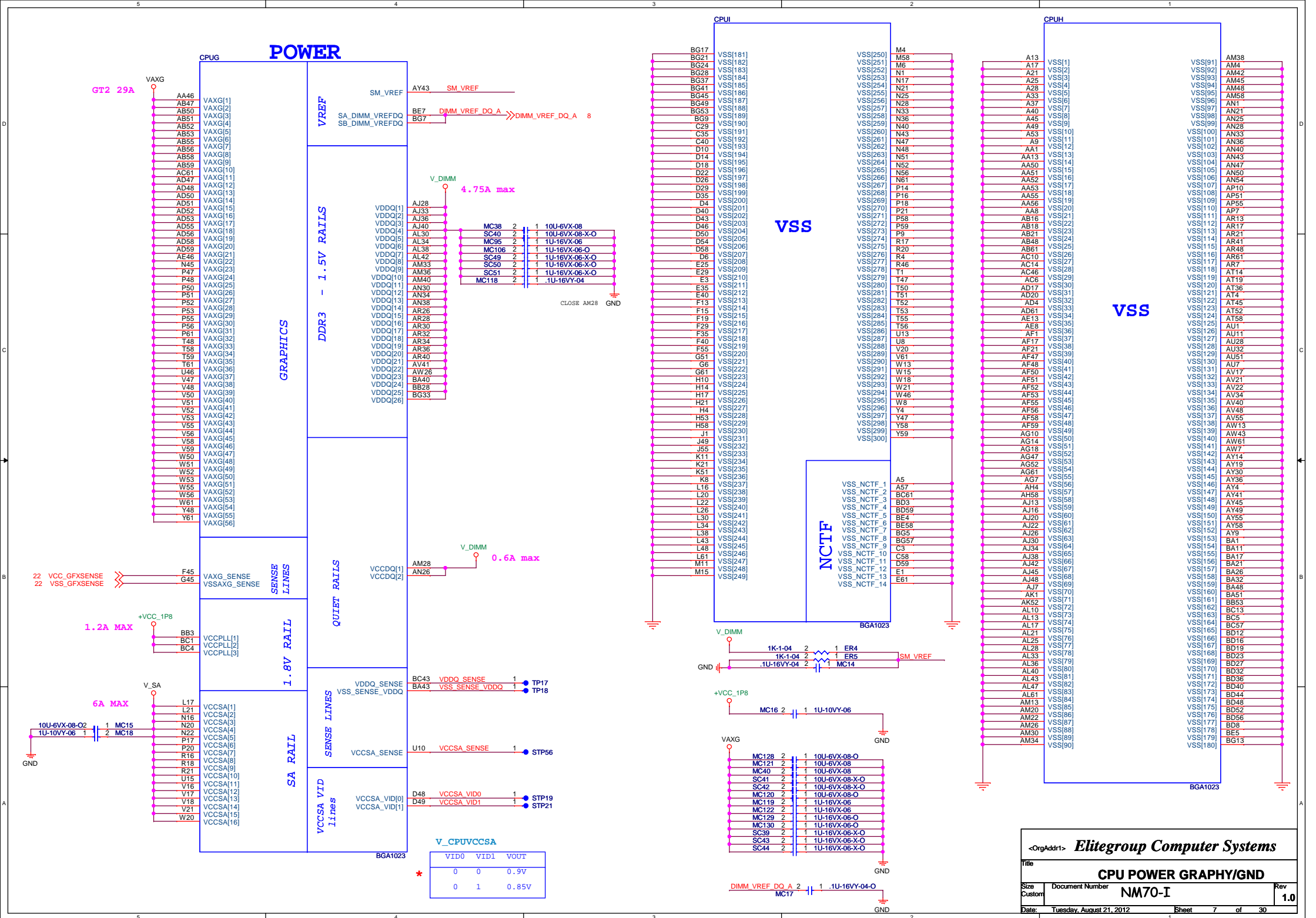
BGA1023



VCCIO_SEL
High-> 1.05V for IVY
Low-> 1.00V for Sandy



<OrgAddr1> Elitegroup Computer Systems		
CPU POWER/VORE/VTT		
Size	Document Number	Rev
Custom	NM70-I	1.0
Date:	Tuesday, August 21, 2012	Sheet 6 of 30



DDR3 - SO_DIMM

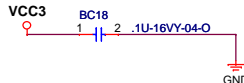
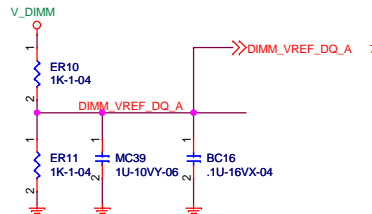
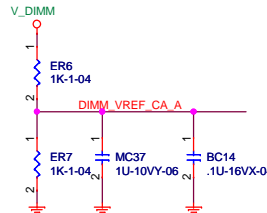
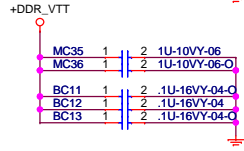
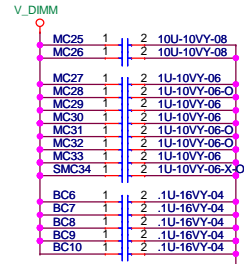
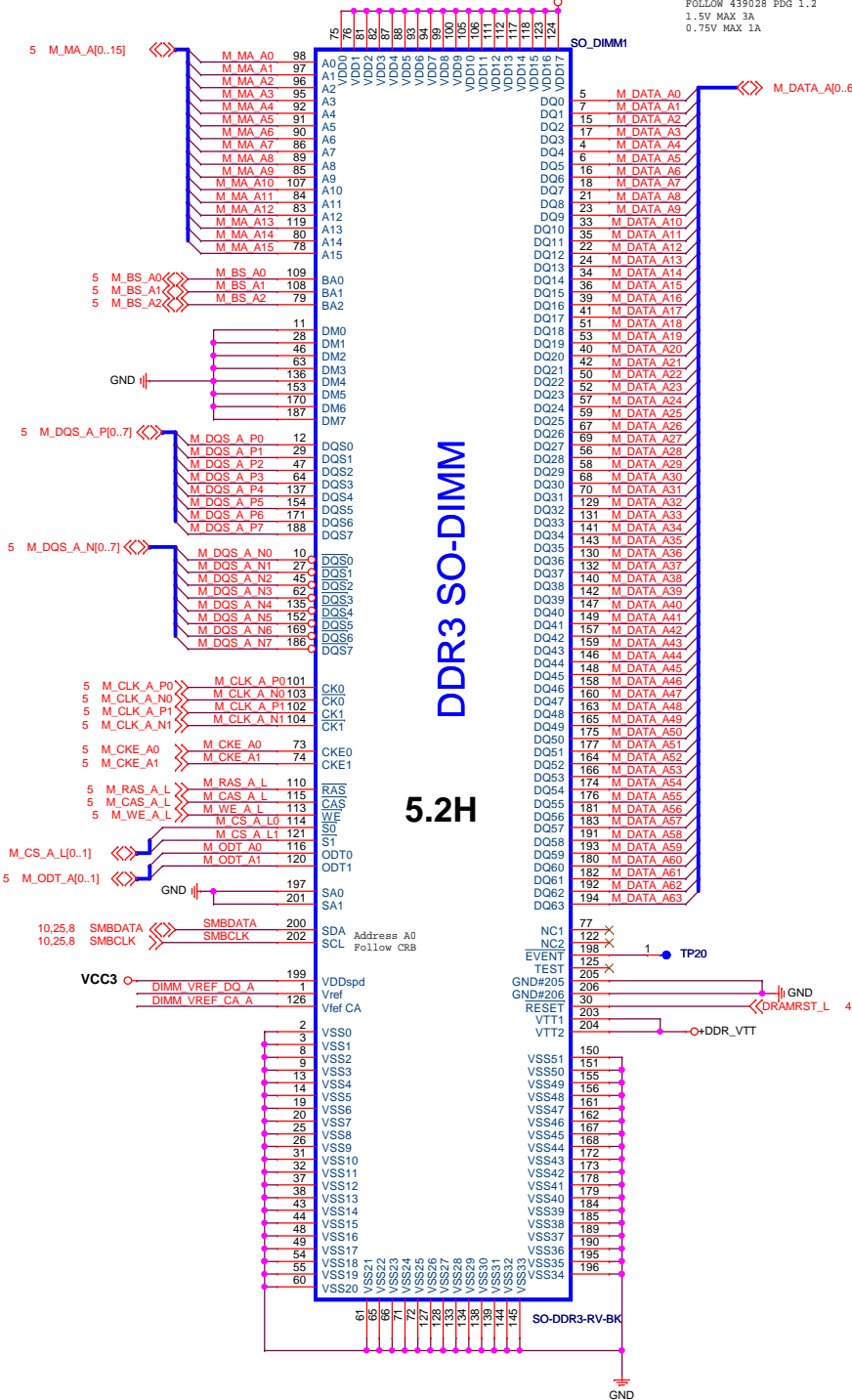
FOLLOW 439028 PDG 1.2
1.5V MAX 3A
0.75V MAX 1A

V_DIMM

SO_DIMM1

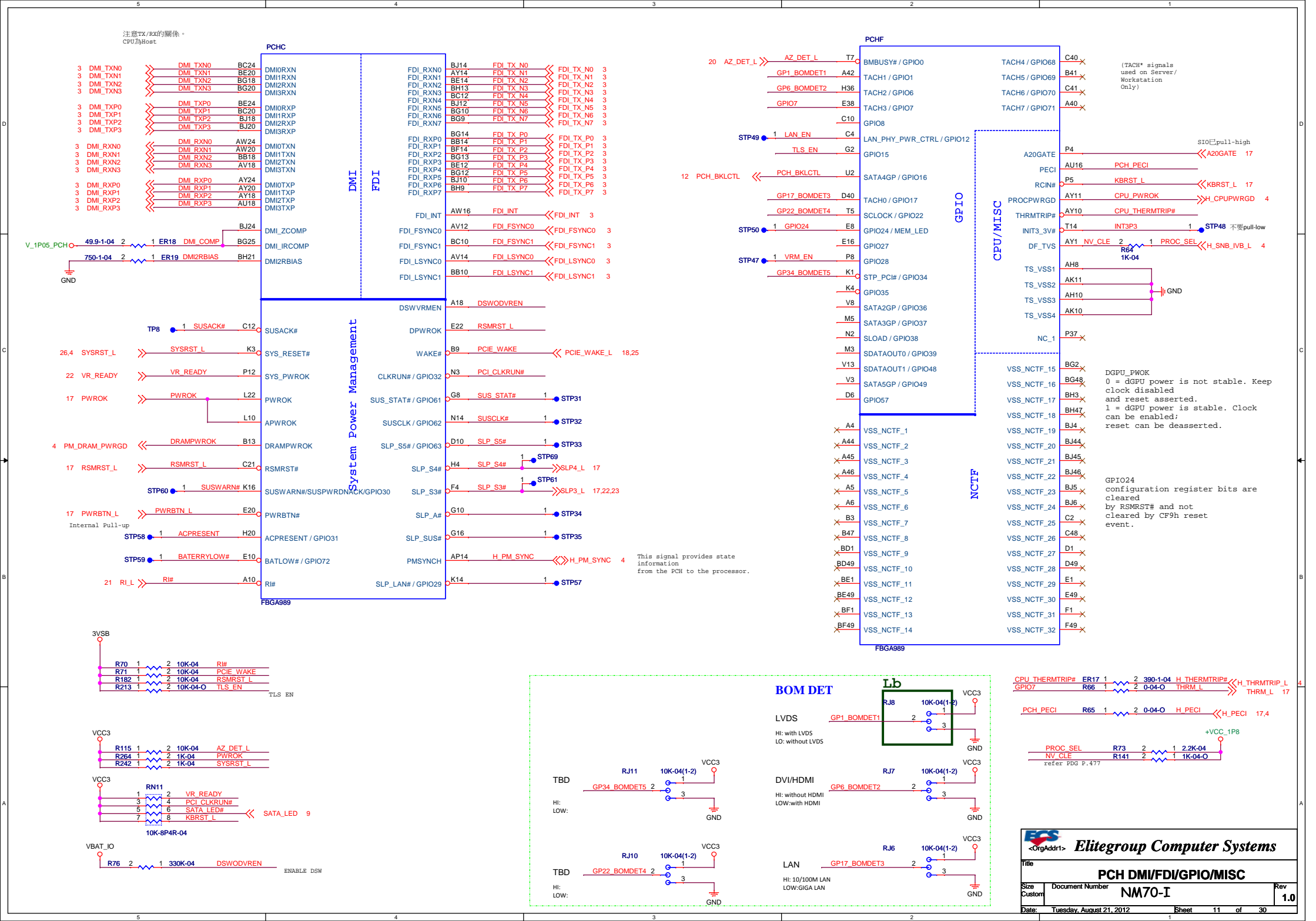
DDR3 SO-DIMM

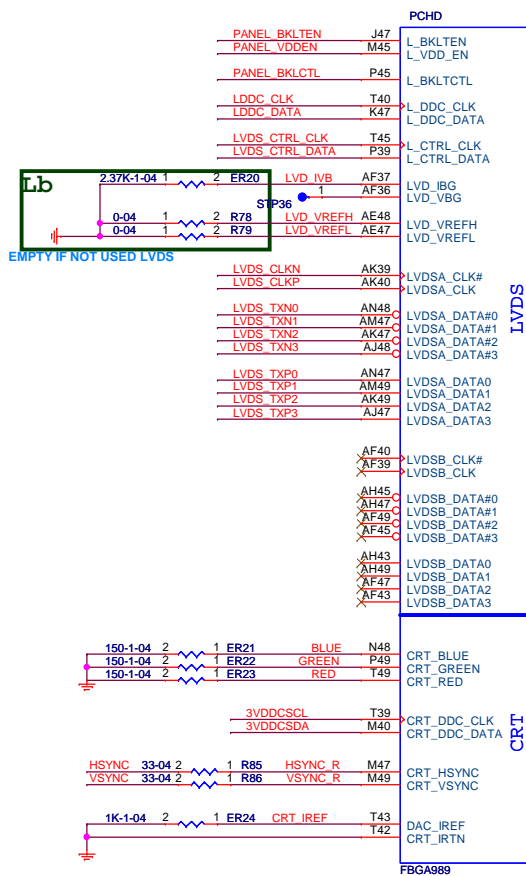
5.2H



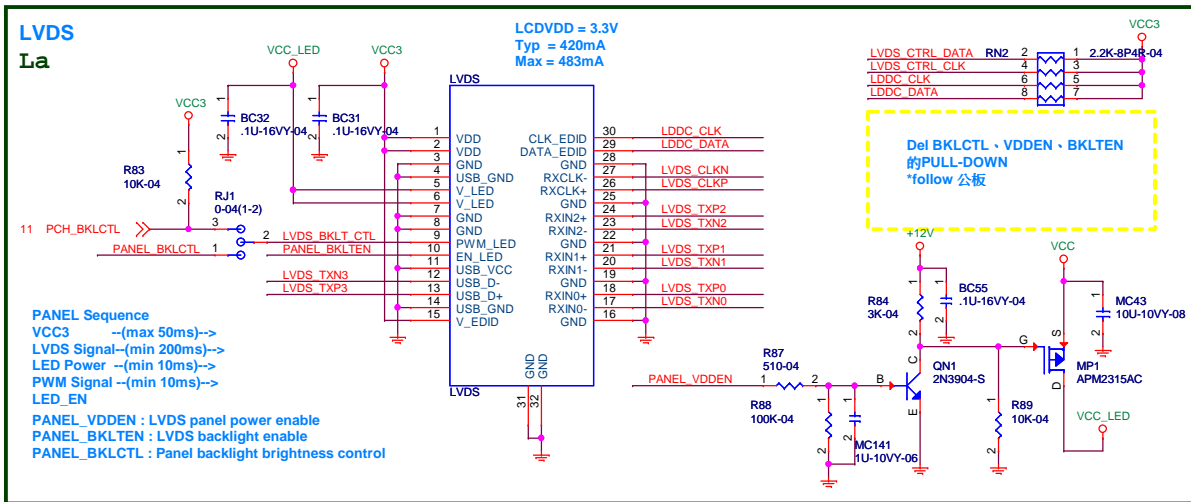
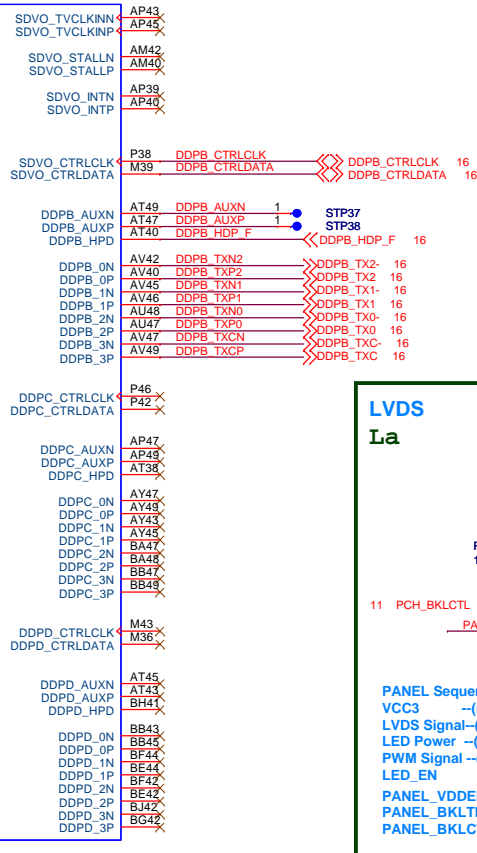
Del Channel B and Change DIMM1 Hight 5.2mm

<OrgAddr1> Elitegroup Computer Systems		
Title DDR3 SODIMM		
Size Custom	Document Number NM70-I	Rev 1.0
Date: Tuesday, August 21, 2012	Sheet 8	of 30





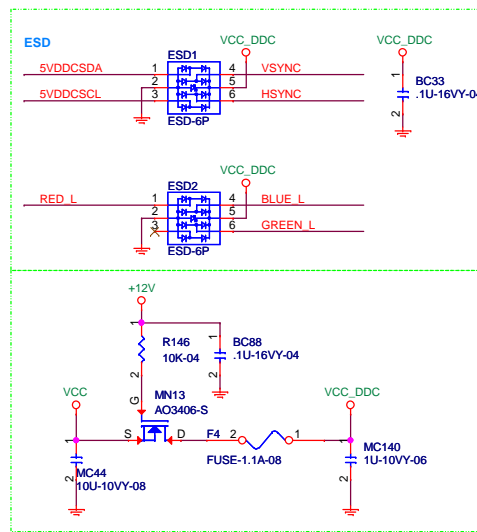
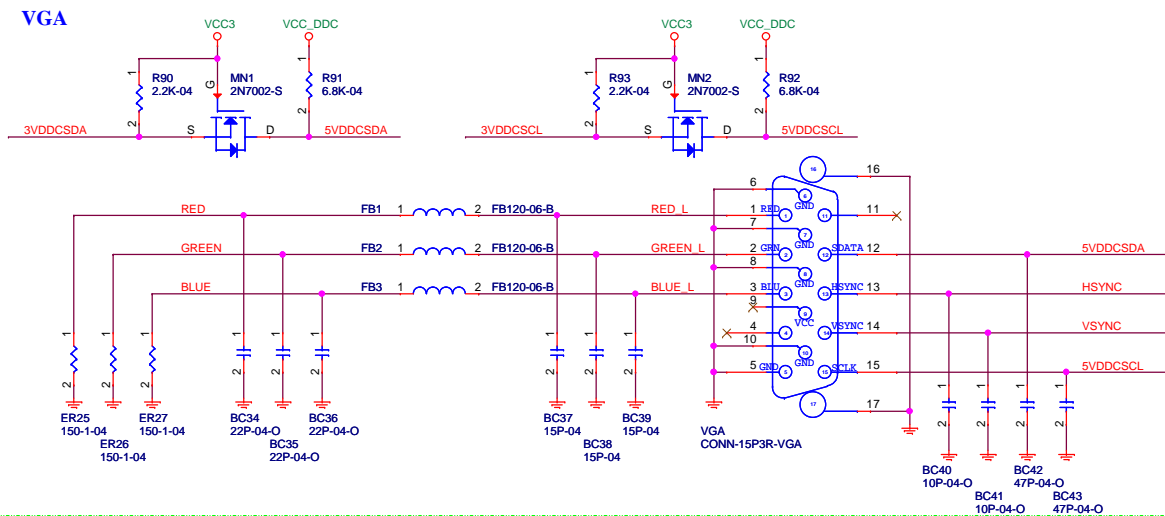
Digital Display Interface

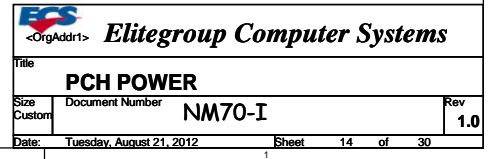


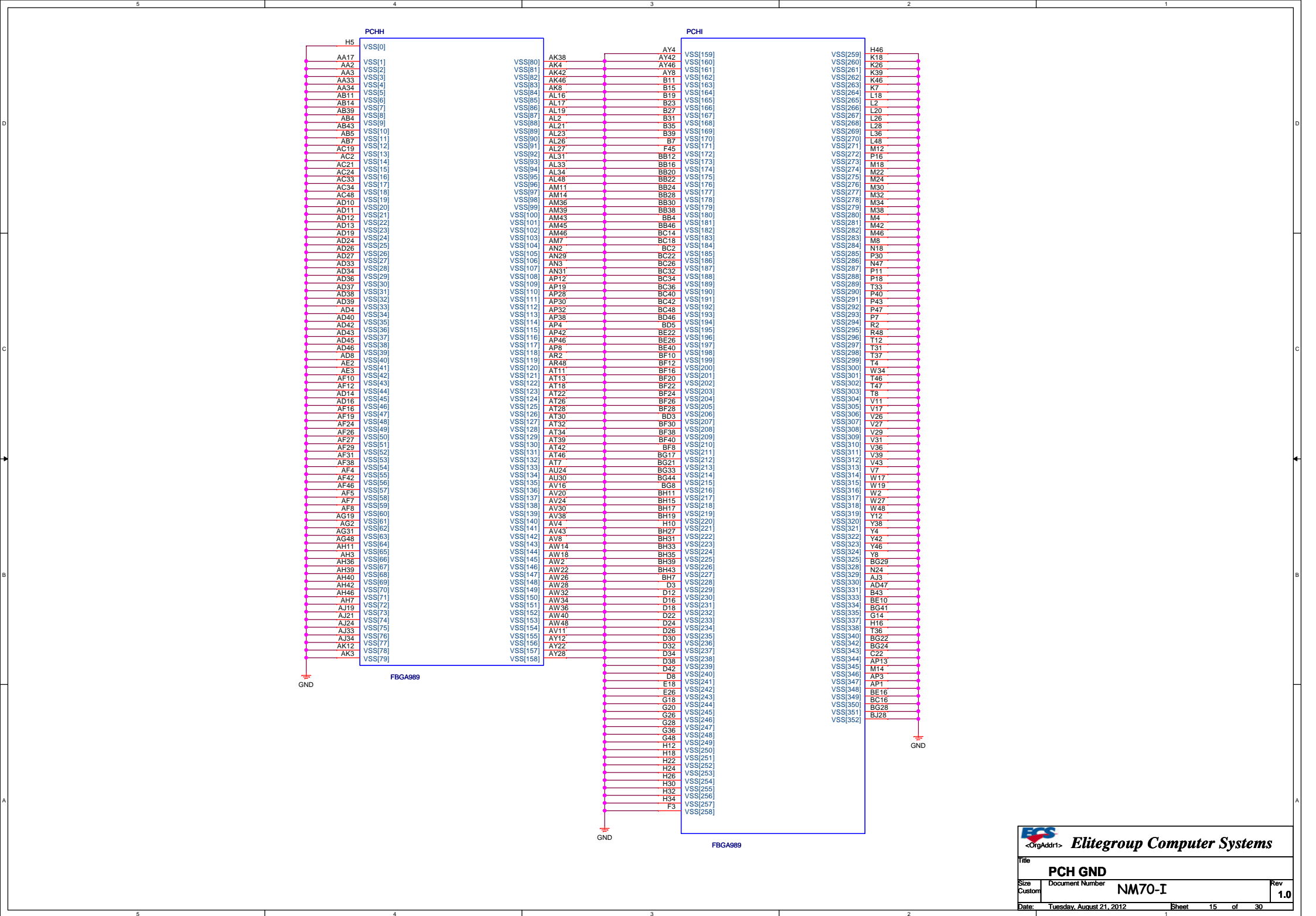
Port	Strap	How to Enable Port?	How to Disable Port?
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2K ohm	No Connect
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2K ohm	No Connect
Port D	DDPB_CTRLDATA	PU to 3.3V with 2.2K ohm	No Connect

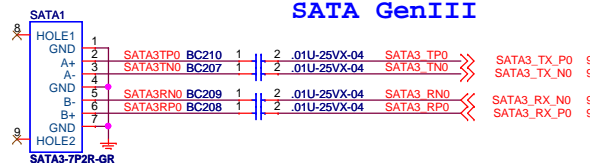
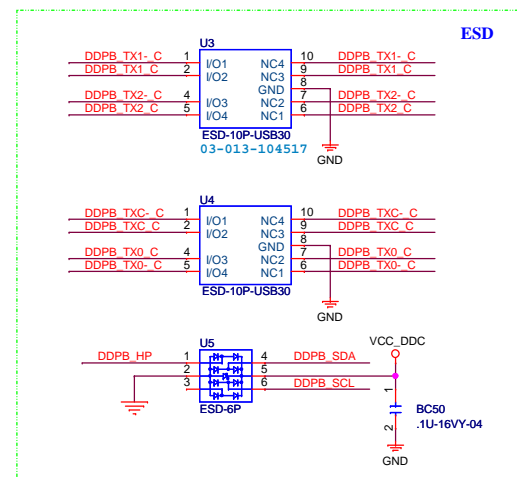
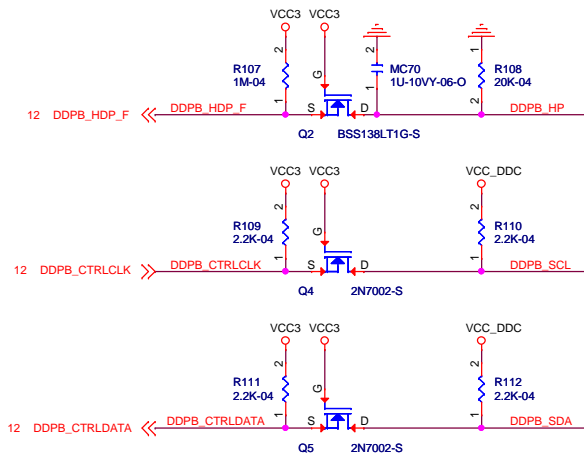
LVDS BOM Difference

	W/ LVDS	W/O LVDS
L _a	V	X
L _b	V	X
L _c Page14	FB19:FB600-06 BC120:10U-16VY-04	BC120:0-04
L _d Page12	10K-04(1-2)	10K-04(2-3)



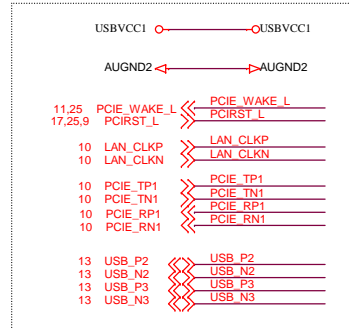




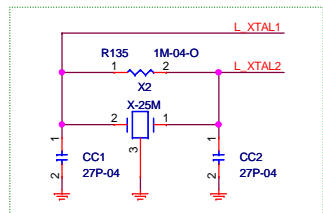
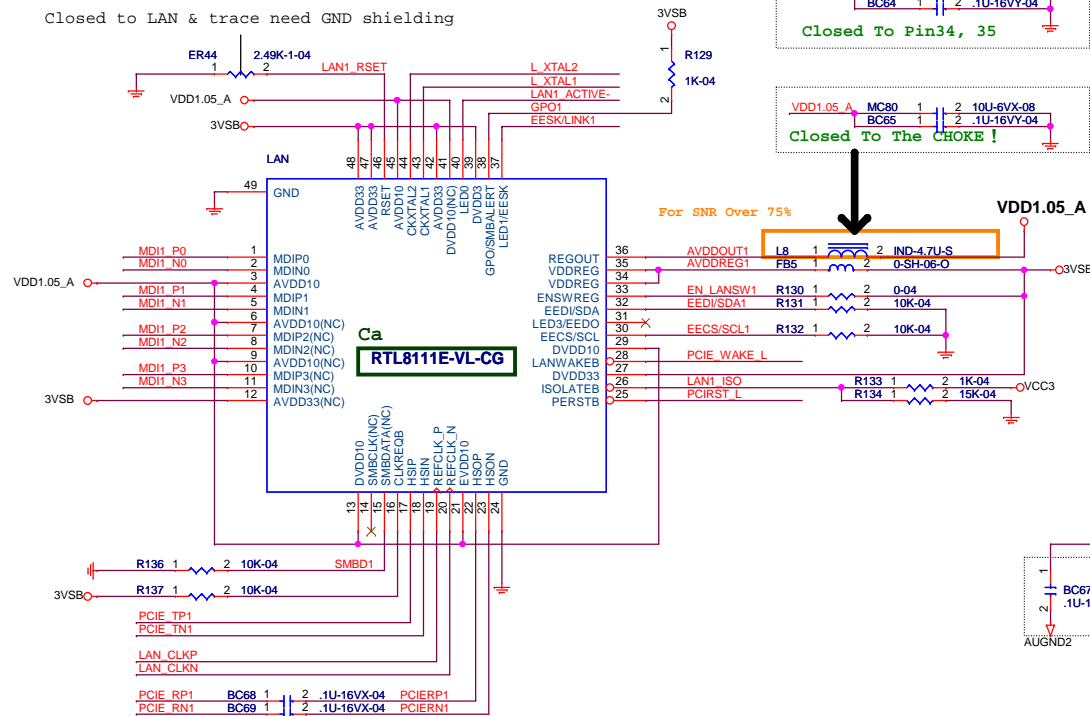


Size Custom	Document Number NM70-I
----------------	---------------------------

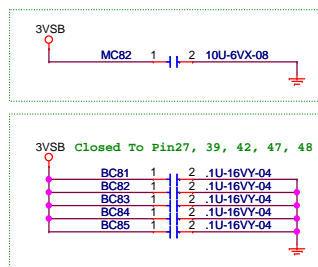
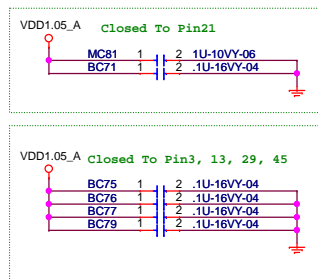
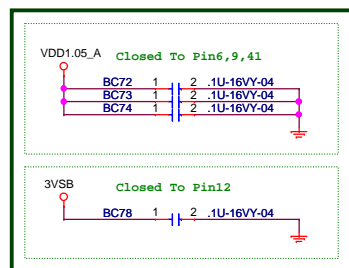
External Connection



Closed to LAN & trace need GND shielding

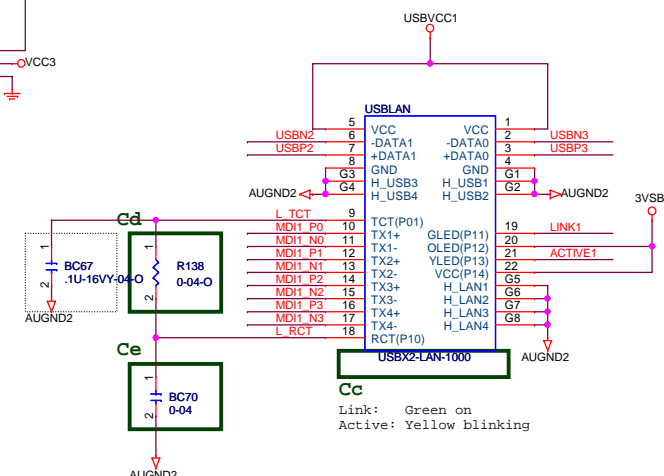
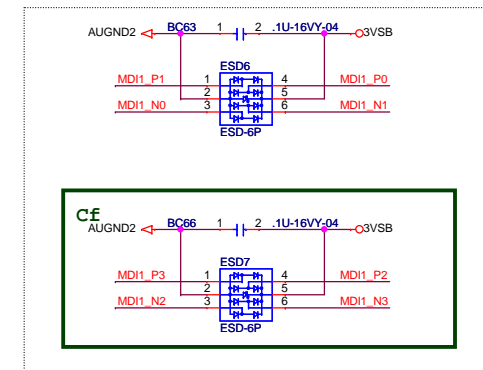


Cb

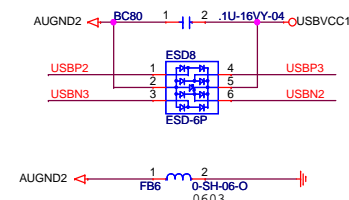


BOM Difference

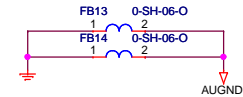
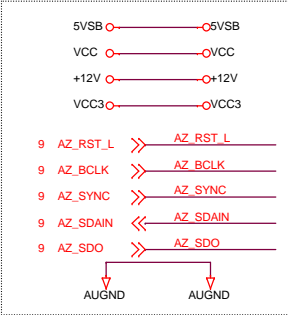
	RTL8111E-GR 1000M	RTL8105E-GR 10/100M
Ca	RTL8111E-VB-GR	RTL8105E-GR
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-25VX-04
Cf	V	X



USB P3 USBP3
USB N3 USBN3
USB N2 USBN2
USB P2 USBP2



External Connection



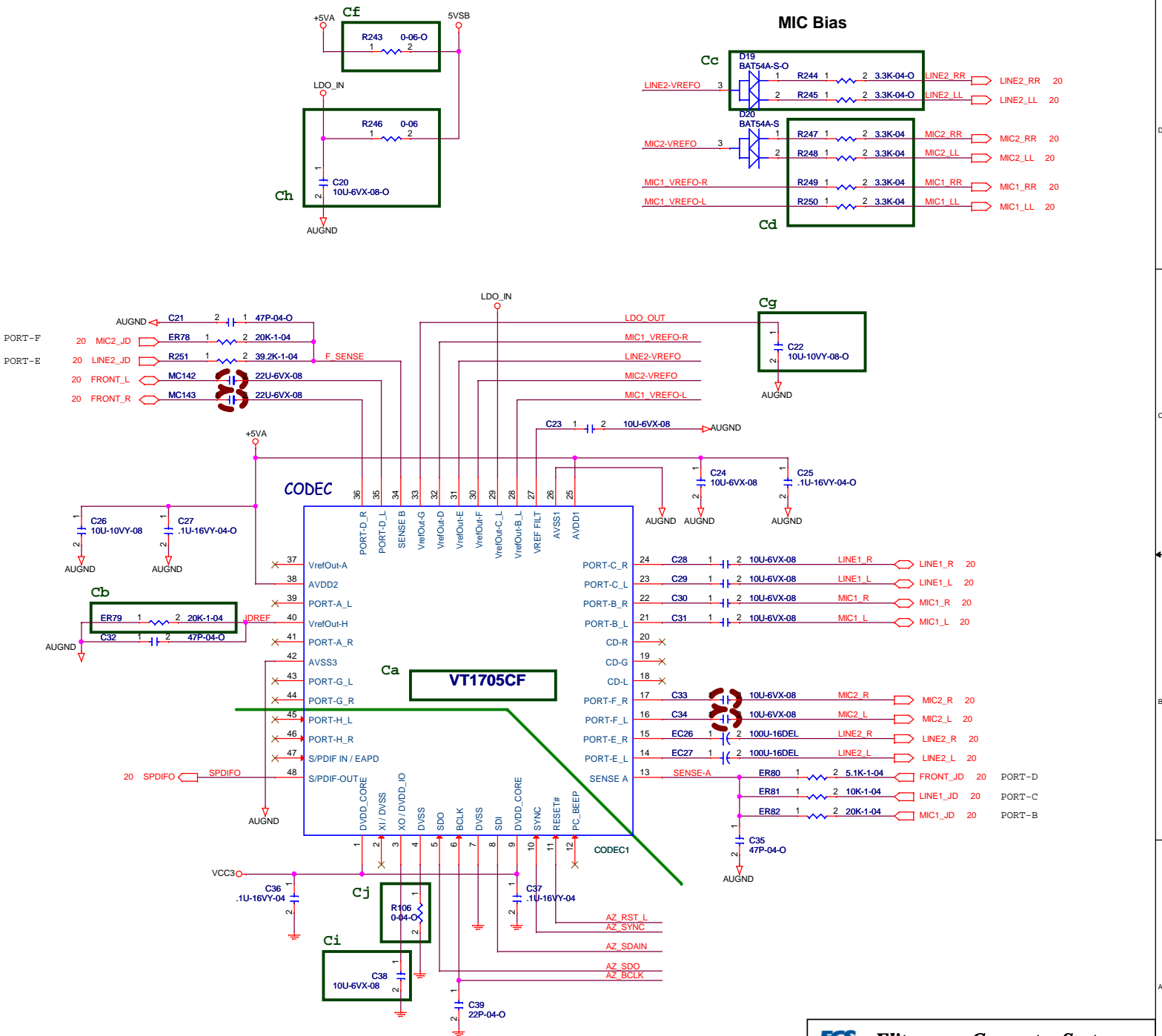
Pin Difference

Pin	ALC662VD	VT1705CE	VT1705CF
2	GPIO0	GPIO0/SPDIF_TX1	GPIO0/SPDIF_TX1/DMIC_CLK
3	REG VREF	GPIO1	REGREF
4	GPIO1	DVSS	GPIO1/DMIC_DATA
25	LDO OUTPUT	LDO VIN	LDO_OUT1
29	LDO VIN	OPTION CAP	LDO_IN
33	LINE1 VREF	LDO OUTPUT	SENSE_C
37	FRONT VREF ?	NC	VREFOUT_C
38	LDO OUTPUT	LDO VIN	LDO_OUT2
45	DMIC DATA	NC	NC
46	DMIC CLK	NC	NC
47	EADP	EADP	EADP/SPIDF_RX

BOM Difference

Location	ALC662VD	VT1705CE	VT1705CF
Ca	ALC662-VD0-GR	VT1705CE	VT1705CF
Cb	20K-1-04	5.1K-1-04	20K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	16-04	32-04
Cf	X	V	X
Cg	X	V	X
Ch	V	X	V
Ci	V	X	V
Cj	X	V	X

When you change BOM, remember change GPI to inform
B10S use different Verb-Table.



Elitegroup Computer Systems

Title

AUDIO VT1705/ALC662 (CHIP)

Size Custom

Document Number

NM70-I

Rev 1.0

Date:

Tuesday, August 21, 2012

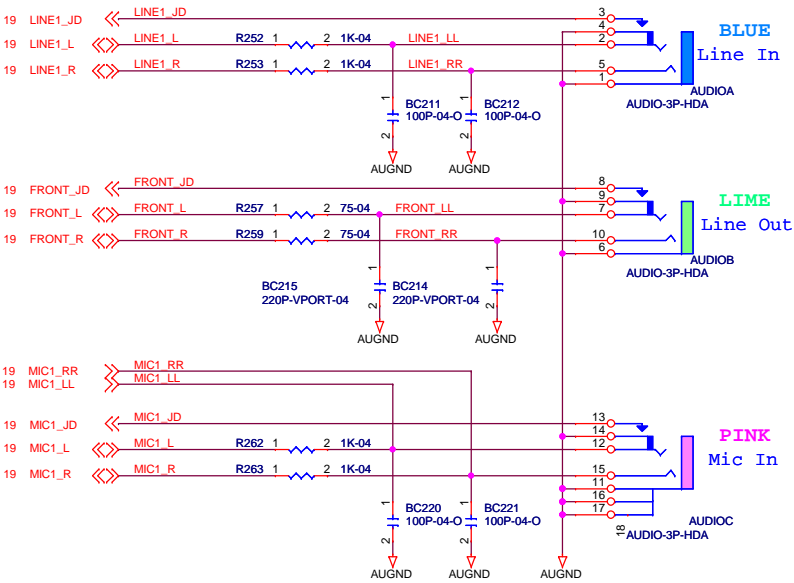
Sheet 19 of 30

External Connection

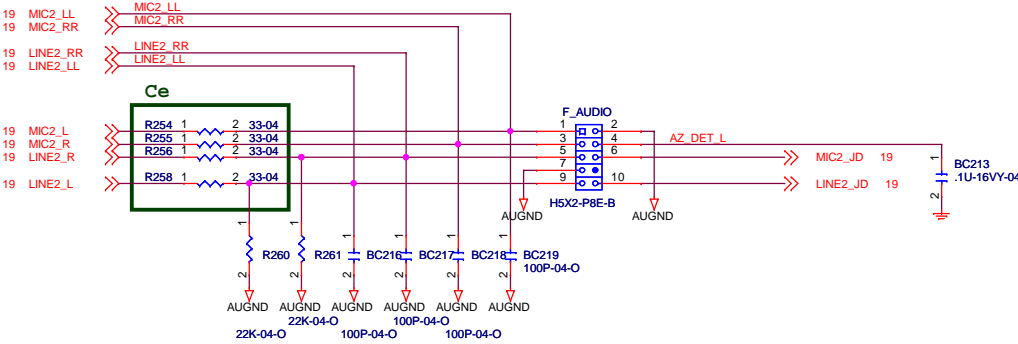


* AZ_DET_L connect to PCH GPIO 0
for AC97 Panel support

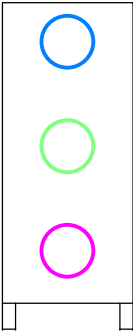
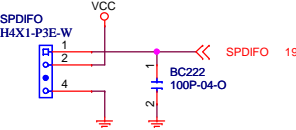
REAR-AUDIO



FRONT-AUDIO



SPDIF-OUT

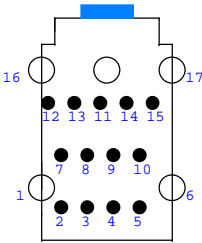


FRONT VIEW

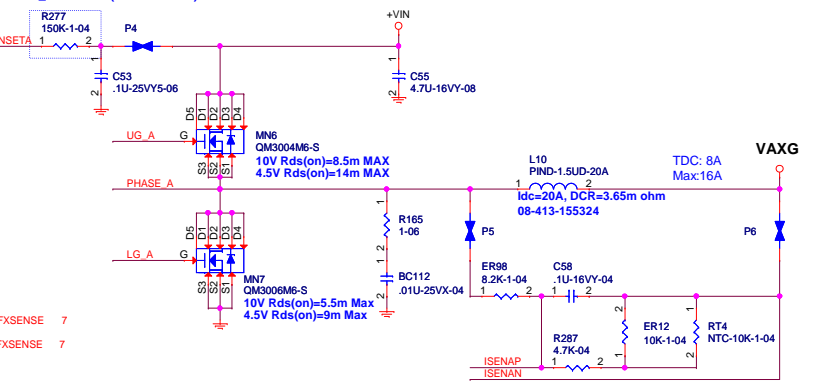
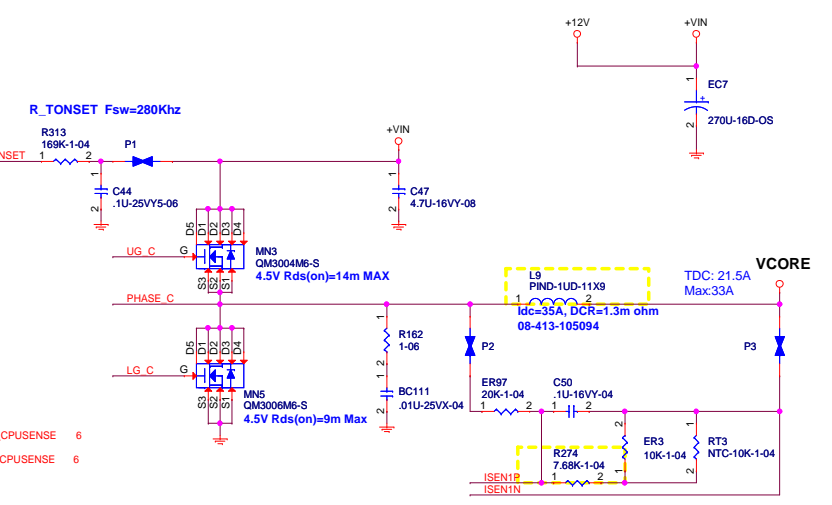
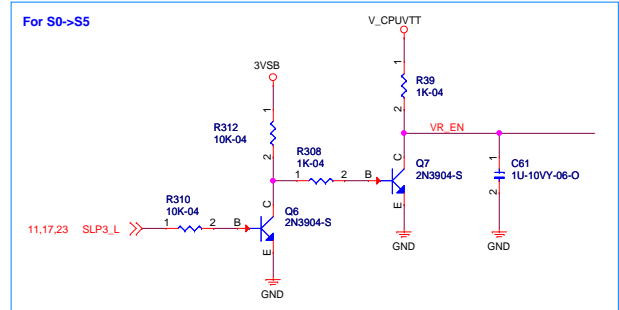
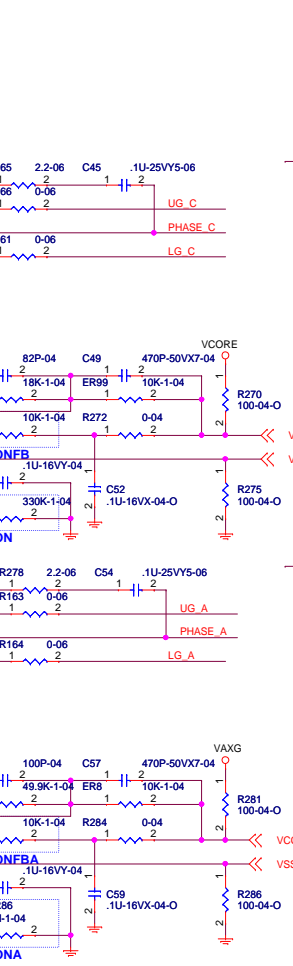
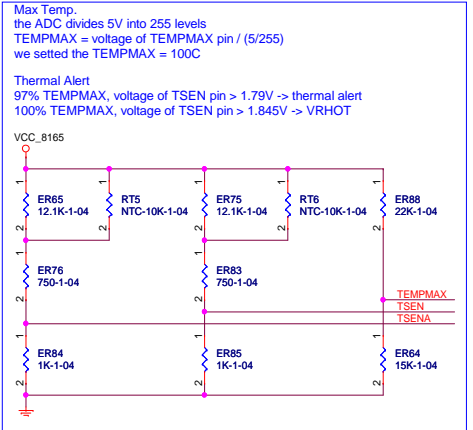
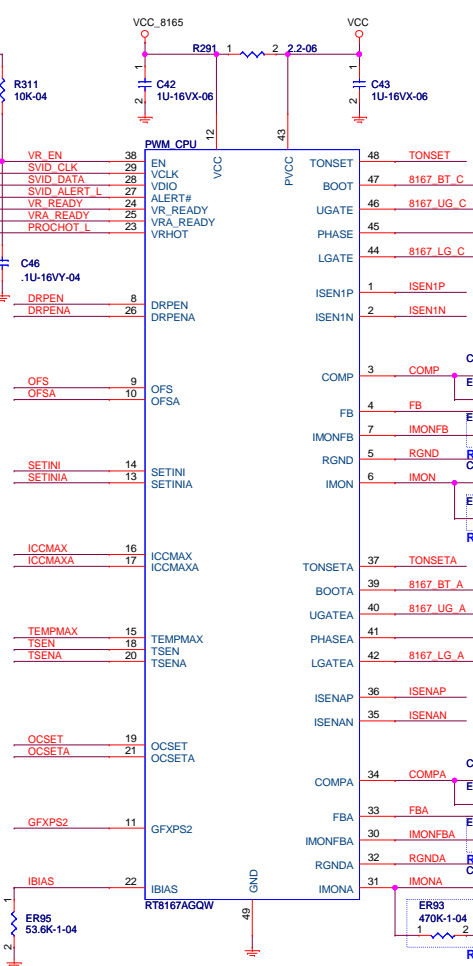
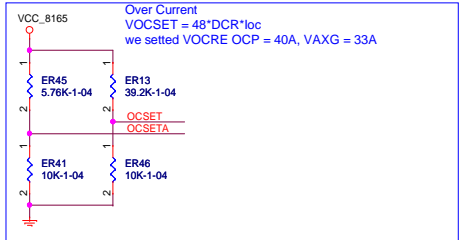
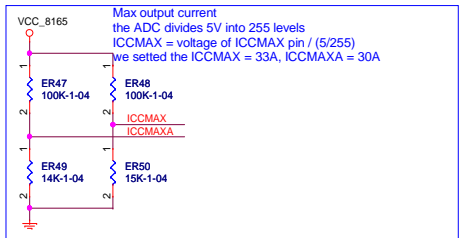
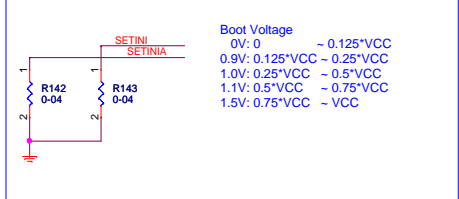
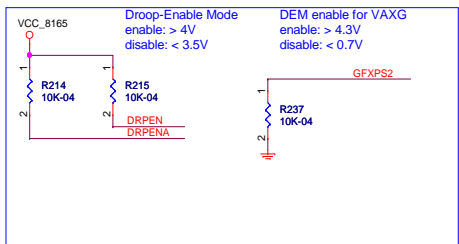
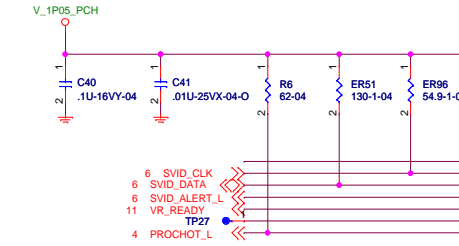
Line in

Front out

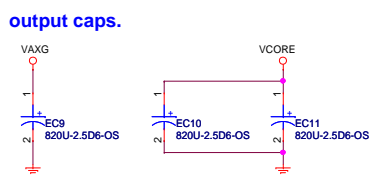
Mic in



TOP VIEW



ER13 39K
ER45 5.8K
ER90 345
R313 170K
R274 7.6K

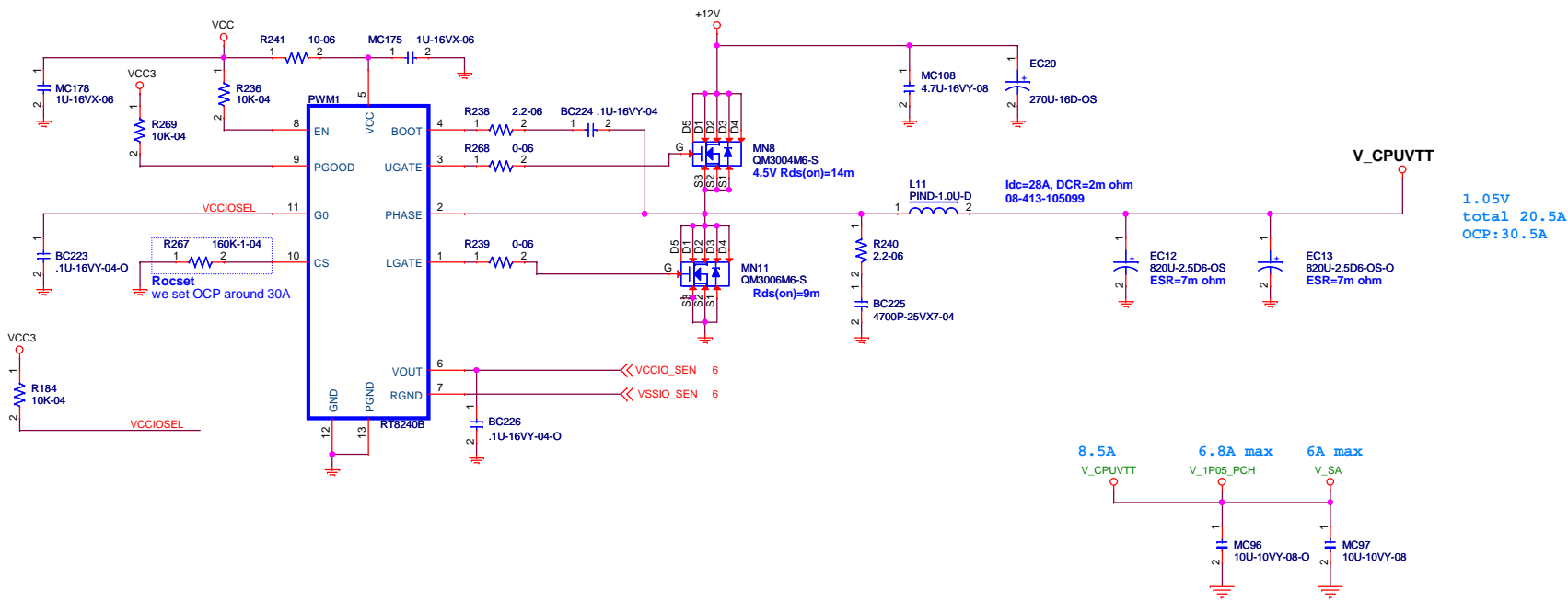


External Connection



VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V *

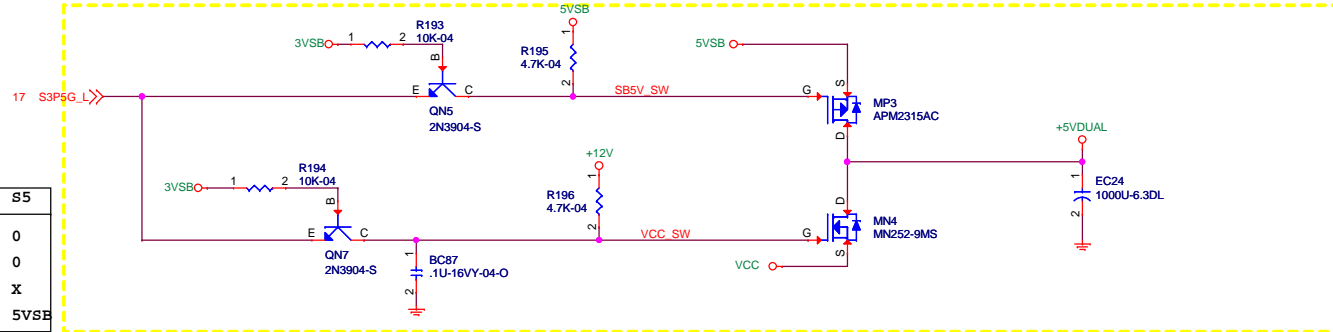
$$OCP = 2 \cdot Vocset \cdot R176 \cdot \frac{1}{DCR} \cdot \frac{1}{Radj}$$



1.05V
total 20.5A
OCP: 30.5A

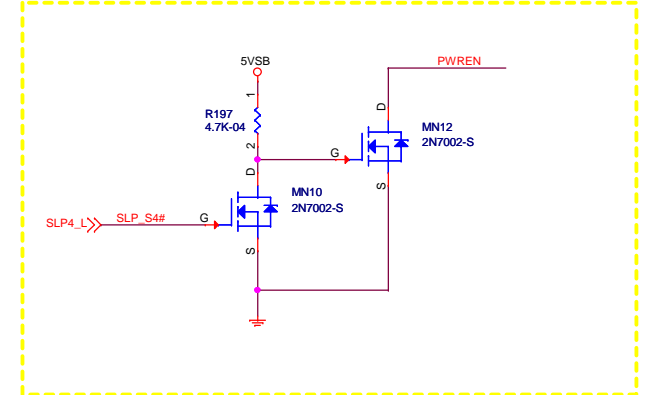
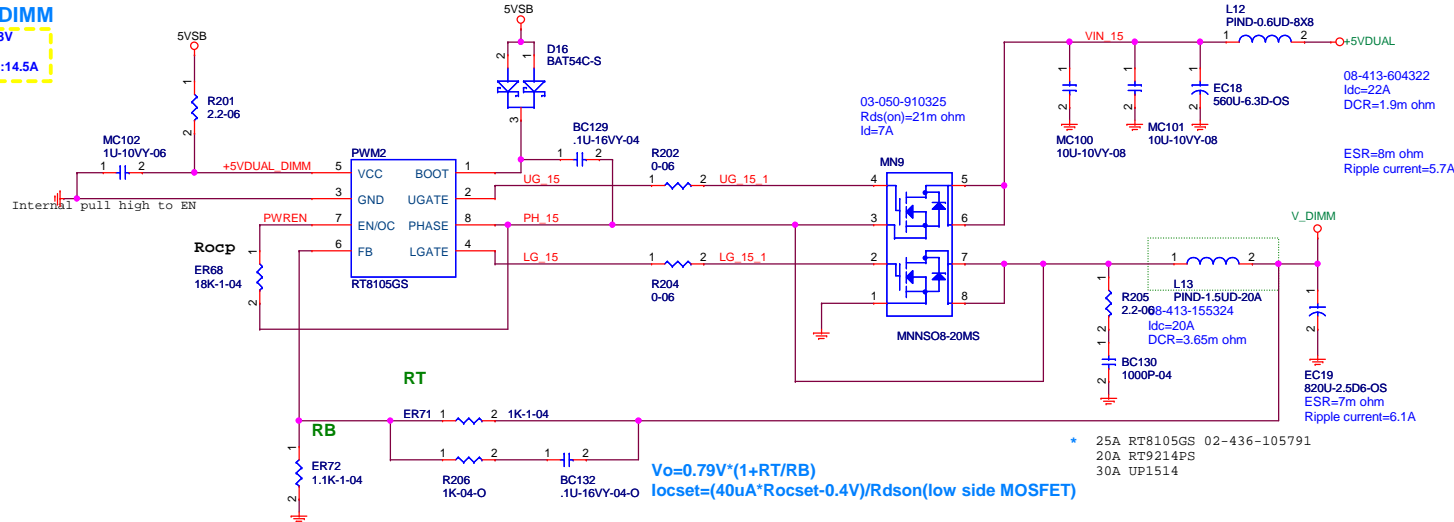
5VDUAL

S0	S3	S5
S3P5G_L 1	0	0
U-P	X	0
U-N	0	X
5VDUAL	VCC	5VSB



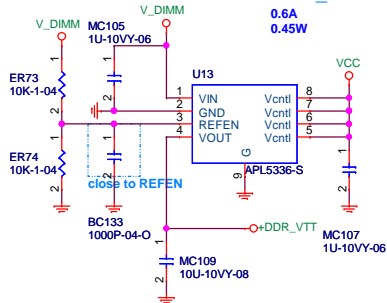
V_DIMM

1.508V
8.3A
OCP:14.5A



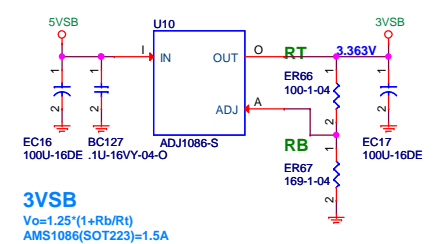
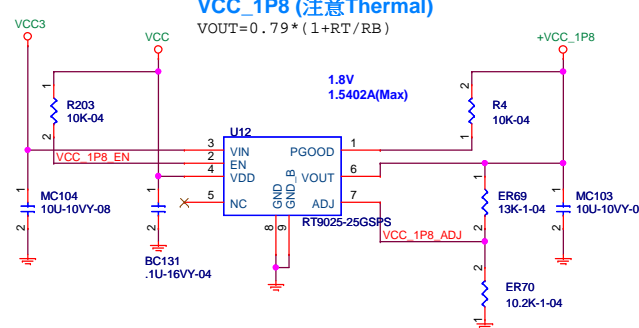
DDR_VTT

0.6A
0.45W

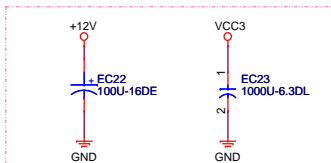
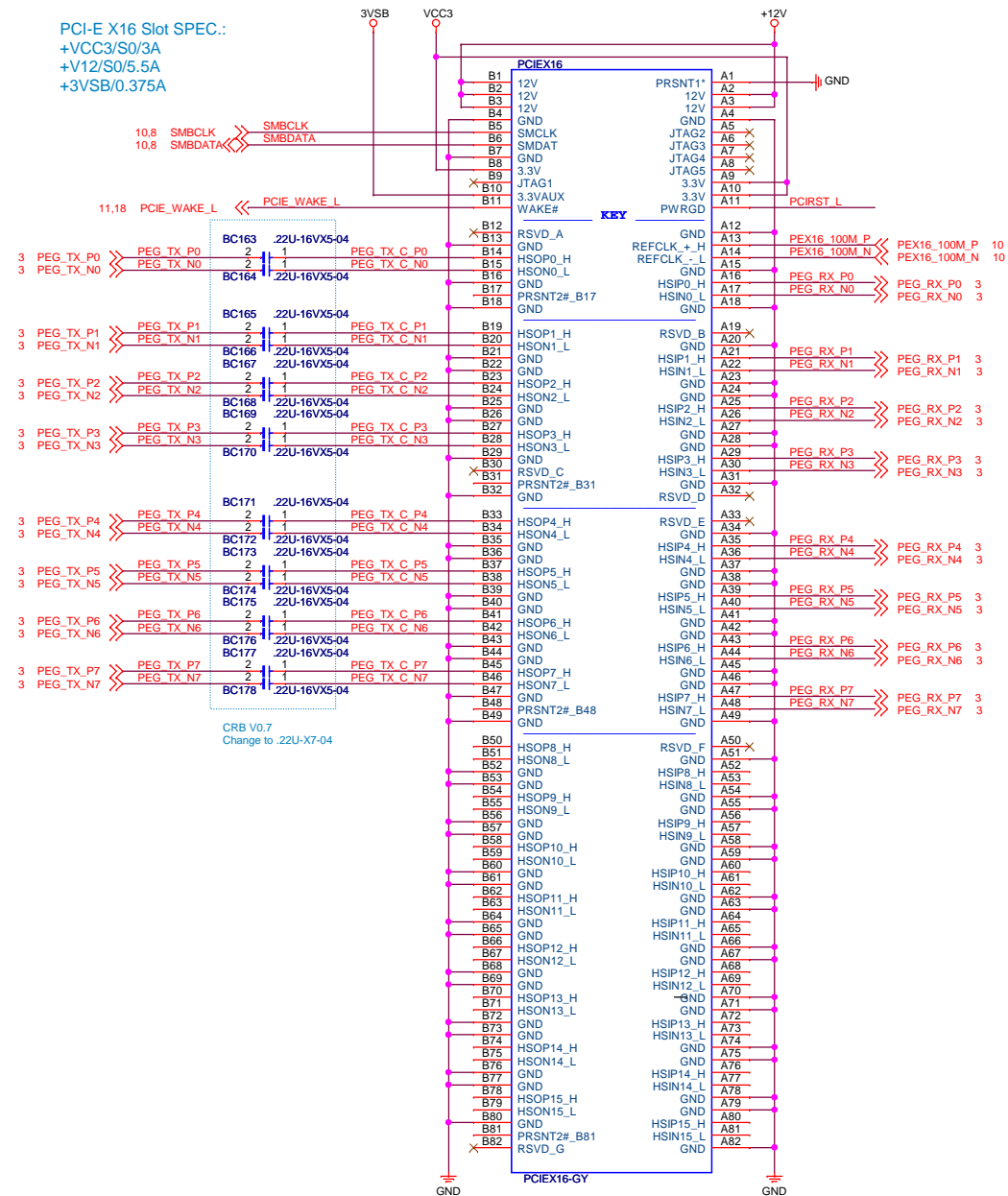


VCC_1P8 (注意Thermal)

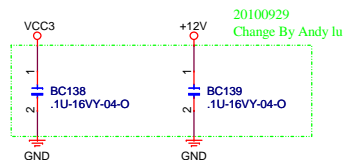
$V_{OUT} = 0.79 * (1 + RT/RB)$



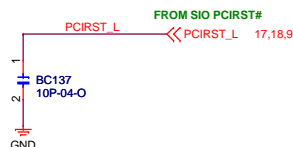
PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A



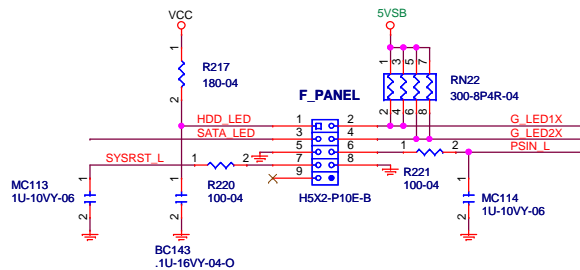
Between PEX16 & PEX1A



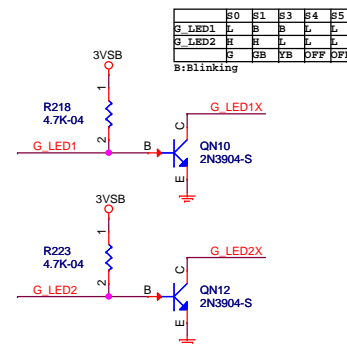
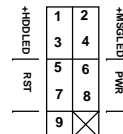
20100929
Change By Andy lu



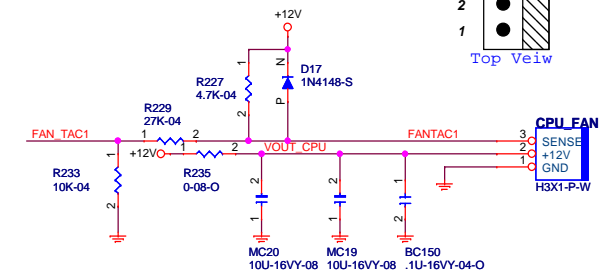
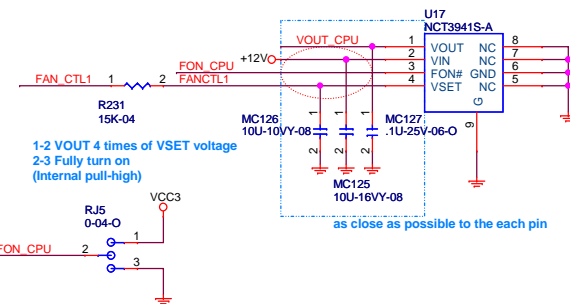
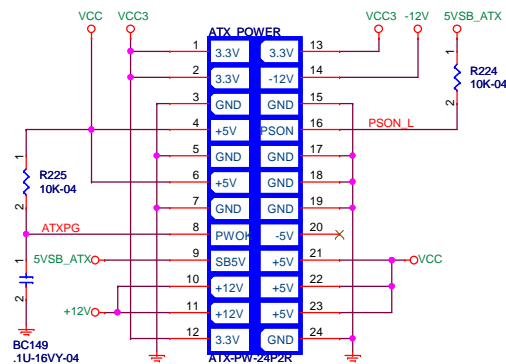
FRONT PANEL External Connection



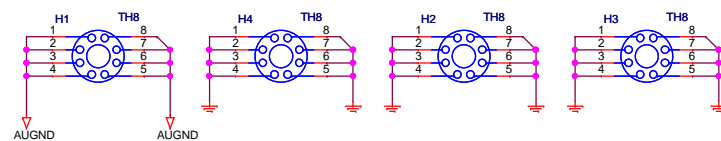
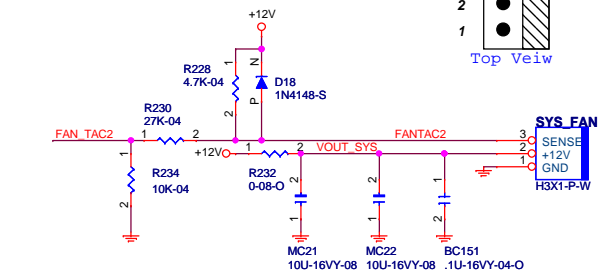
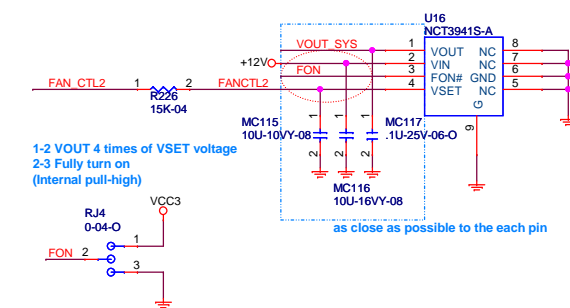
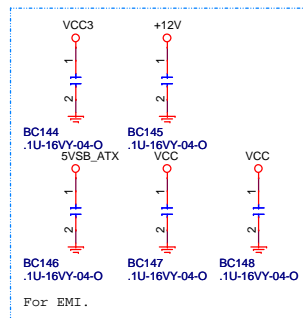
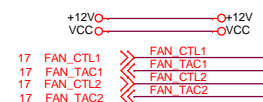
F_PANEL



POWER CONNECTOR External Connection



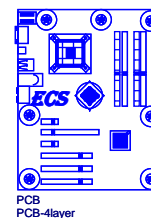
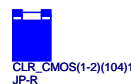
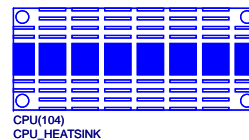
FAN External Connection



USBPWR_R(1-2)(104)



USBPWR_F(1-2)(104)



Elitegroup Computer Systems

Front Pan/FAN/PowerConn

Size Custom Document Number NM70-I Rev 1.0

Date: Tuesday, August 21, 2012 Sheet 26 of 30

Panther Point

Name	Type	Voltage	Default	Functional Description
GPIO0	I	VCC3	Input	AZ_DET_L
GPIO1	I/O	VCC3	Input	BOM DET1 * HI: With LVDS LOW: Without LVDS
GPIO6	I/O	VCC3	Input	BOM DET2 * HI: HDMI LOW: DVI
GPIO7	I	VCC3	Input	THRM_L
GPIO16	blink	VCC3	Input	BKLCTL
GPIO17	I/O	VCC3	Input	BOM DET3 * HI: Giga LOW: 10/100
GPIO13	I	3VSB	Input	LPCPME_L
GPIO22	I/O	VCC3	Input	GPIO22 * HI: W/ COM1 LOW: W/O COM1

F71869

Name	Type	Voltage	Functional Description	Function
GPIO15	I/O	3VSB	Power LED for VSB	G_LED1
GPIO16	I/O	3VSB	Power LED for VCC	G_LED2
OVT#	O			THRM_L
VIN1	I			VIN1 for VCORE
VIN4	I			VIN4 for V_DIMM
FANIN1	I		CPU FAN tachometer	
FANCTL1	O		CPU FAN control	
FANIN2	I		System FAN tachometer	
FANCTL2	O		System FAN control	
S3P5G_L/ST2			S0=1 S3=0 S5=0	

	S0	S1	S3	S4	S5
G_LED1	L	P	S	L	L
G_LED2	H	H	L	L	L
	S	SB	YB	OFF	OFF

B:Blinking

